Design and Performance Analysis of 20nm 7-Fin SOI FinFET

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Abstract: Scaling of standard CMOS is becoming difficult due to rising subthreshold leakage and gate leakage. FinFETs i.e. Multi-gate FETs have come out as the most assuring contenders to extend the scaling of CMOS insub-25nm region this is because of more electrostatic control due to use of multiple gatesover the channel which lowers the coupling between drain and source in the subthreshold regime. Driving capability is increased for low voltage designs by using SOI FinFETs. In this paper, designing and performance analysis in terms of V-I characteristics of 20nm 7-fin SOI FinFET is discussed..

Keywords: SOI (Silicon-on-Insulator); FinFET; I_{on}(drain ON current); I_{off} (drain OFF current); CMOS; Multi-gate FET; TCAD (Technology Computer Aided Design).

Introduction

MOSFET (metal-oxide semiconductor field-effect transistor) is voltage controlled field effect transistor. From *source side,*charge carriers enter the channeland leave through the *drain.* The voltage on gate electrode controls the width of the channel and gate is located between drain andsource. And a thin layer of metal oxide acts as an insulator between gate and channel.A FinFET is a type of multi-gate MOSFET. A multi-gate transistor is a transistor which has more than one gate and silicon film is wrapped over the channel to form the body andFinFET is so called because its structure looks like a set of fins.The thickness of device defines the channel length which isthe distance between the drainand source junctions. To fabricate fast and compact devices channel length has been constantly reduced. Reduction in channel length leads to the increase in short channel effects(SCEs). The SCEs are attached to two physical phenomena; a) The limitation enforced on electron drift characteristics in the channel. b) The shortening of channel length leads to threshold voltage modification.FinFET has emerged as a perfect solution for these problems.

Literature Review

In CMOS, the high gate and subthreshold leakage are there when gate length is reduced beyond 25 nm due to increased short channel effects therefore the need of multi-fin FinFETarises. Multi-fin FinFET provide more control due to presence of multiple gatesover channel which results in reduction of short channel effects and decrease in off current.The effect of number of fins, effect of number of gates, gate space to contact effect, fin space effect of different processeshas been discussed [1].The important parameters like drain currents (I_{on} and I_{off}), SS and threshold voltage for 3D SOI double gate FinFET, Tri-gate FinFET and Independent gate FinFET using TCADwere examined. Also, using high-K dielectric drain current was optimized and analysed over various gate lengths [2].The capacitive effect of multi-fin FinFET with the help of TCAD simulations have been investigated. The analysis for capacitance change was performed in 32nm FinFET for various fin pitch and height [3].The increase in layout-dependent effects due to increasing stress engineering were explored. They discussed the STI induced stress on gate position along fin and fin length [4]. The Multi-fin bulk SiFinFET design problems and issues using 3D numerical simulation were discussed[5].The effects of fin structure and the number of fins on the device DC and dynamic behaviour, and random doping produced characteristic variations of FinFETs have been discussed [6].

Device Design And Methodology

This device is designed and analyzed in terms of V-I characteristics using Cogenda Visual TCAD (Technology Computer Aided Design). Table 1 shows the dimensions and material used for various regions and indicates doping concentration of source, drain, substrate and fins.

Table 1: Dimensions and Material for different regions of Multi-Fin FinFET

Region	**Dimension**	**Material**
Source	25nm	Si (Uniform, Donor, 1e+19)
Drain	25nm	Si (Uniform, Donor, 1e+19)
Gate	20nm	W(tungsten)
Oxide on Gate	2.8205nm	HFO_2
Spacer	4nm	Nitride
Fin	Fin height-30nm Fin width-6.8nm	SiGe (Uniform, Acceptor, 1e+15)
Substrate	Substrate height-70nm	Si (Uniform, Acceptor, 1e+15)
Oxide (on either side of fin)	2.5nm	SiO_2

Result And Discussion

20nm 7-fin SOI FinFET is implemented using Cogenda Visual TCAD. And its V-I characteristics i.e. Transfer characteristics (V_{gs} vs I_d) and Output Characteristics (V_{ds}vs I_d) are simulated.Fig.1 and Fig.2 shows the Structure of 20nm 7-fin SOI FinFET.

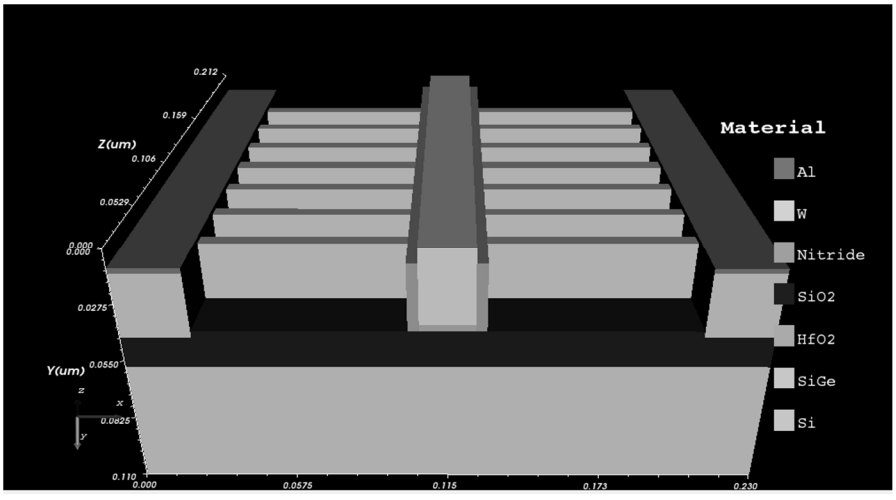

Fig.1: Structure of 20nm 7-fin SOI FinFET (side view)

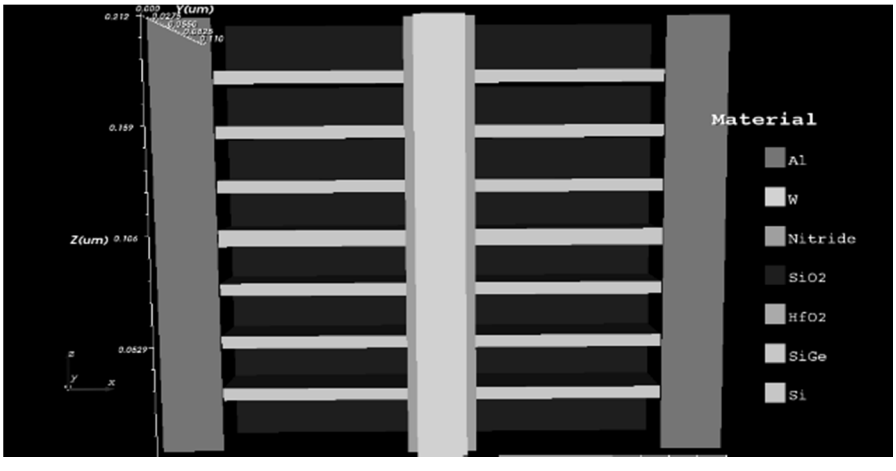

Fig.2: Structure of 20nm 7-fin SOI FinFET (top view)

From V-I characteristics,I_{on}, $I_{off}$is obtained and thenI_{on}/I_{off}ratio is calculated from that.I_{on} is calculated at V_{gs}=1V and $I_{off}$is calculated at V_{gs}= 0V at constant drain voltage of V_{ds}= 0.1V. Table 2 indicates the value of I_{on}(drain ON current),I_{off} (drain OFF current) and I_{on}/I_{off} ratio.

Table 2: FinFET parameters and their values

Parameter	Value
I_{on}	4.5536e-06
I_{off}	2.51489e-10
I_{on} / I_{off} ratio	1.8106e+4

Transfer Characteristics (V_gs vs I_d):

To simulate Transfer characteristics (V_{gs} vsI_d), gate voltage is varied from 0V to 1V with the step voltage of 0.05V and constant voltage of 0.1V is applied to drain. Source terminal is at ground potential. Fig.3 shows the drain current variation with gate voltage. The drain current initially increases very slowly until gate voltage is less than threshold voltage. As gate voltage exceeds threshold voltage, the drain current increases rapidly.

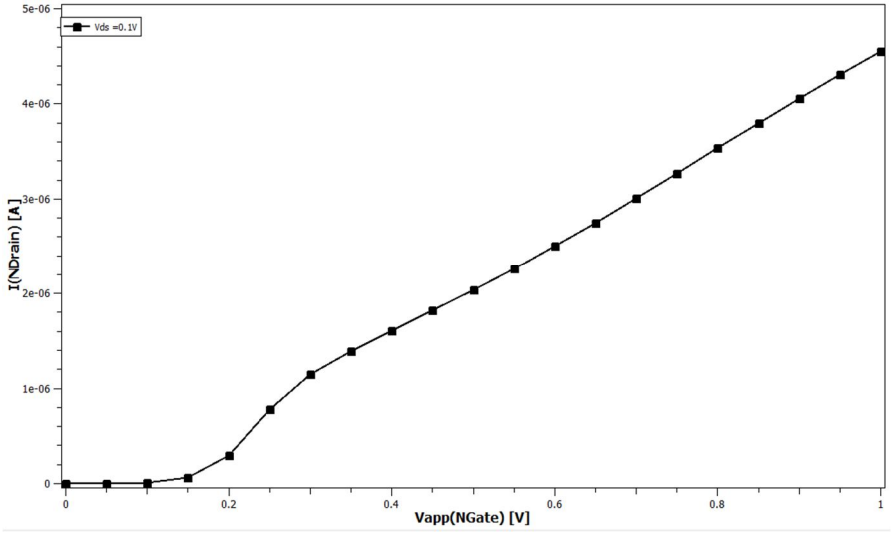

Fig.3: Transfer Characteristics

Output Characteristics (V_{ds} vs I_d):

To simulate Output characteristics (V_{ds} vs I_d), drain voltage is varied from 0V to 1V with the step voltage of 0.05V and constant voltage of 0V, 0.5V,1V,1.5V and 2V is applied to gate. Source terminal is at ground potential.Fig.4 shows the drain current variation with drain voltage at different gate voltages**.**

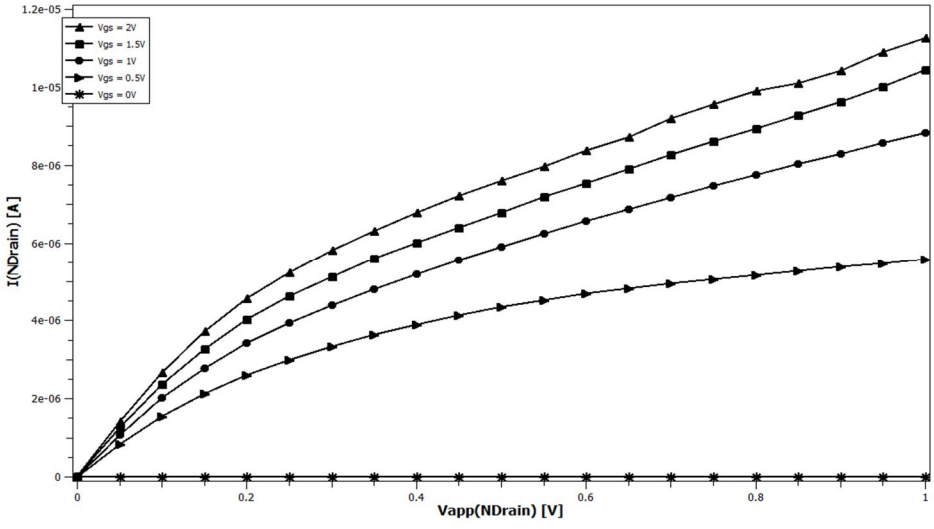

Fig.4: Output Characteristics

Conclusion

20nm 7-fin SOI FinFET is designed and analyzed in terms of V-I characteristics using CogendaVisual TCAD.Also I_{on} , I_{off} is obtained from V-I characteristics and I_{on}/I_{off}ratio is calculated. The value of I_{on} and I_{off}came out to be 4.5536e-06 and 2.51489e-10 and thus calculated value of $I_{on}/I_{off}$is 1.8106e+4.

Future Scope

Future scope of FinFET include further scaling down to 14/16nm and 10nm and Quantum Density Gradient Model can be used for obtaining better V-I characteristics. The optimization of the transistor fin will play a crucial role in this development.Various soft computing algorithms can be used for optimization. Also the different shapes of fin can be used like triangular, trapezoidal etc.

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